

WHAT IS CLAIMED IS:

- 1 1. A multiprocessor system comprising:
2 two or more processor elements whose performances
3 are to be executed by a common program;
4 a control section for switching such plural
5 processor elements one from another for execution by
6 said common program; and
7 a storing section, responsive to each switching
8 of said processor elements by said control section,
9 for storing handover information relating to the
10 common program which information is to be handed over
11 from said one processor element to said another
12 processor element.
- 1 2. A multiprocessor system according to claim 1,
2 wherein, with the switching of said processor elements,
3 said control section stores said handover information
4 from said one processor element into said storing
5 section and then stops the performance of said one
6 processor element and, at the same time, starts the
7 performance of said another processor element using
8 said handover information stored in said storing
9 section.
- 1 3. A multiprocessor system according to claim 1,
2 wherein, if a performance requested to be executed
3 for one of said plural processor elements is to be

4 made by another processor element, said last-named
5 one processor element outputs a switching request
6 signal to said control section for switching said
7 processor elements from said last-named one processor
8 element to the last-named another processor element.

1 4. A multiprocessor system according to claim 2,
2 wherein, if a performance requested to be executed
3 for one processor element is to be made by another
4 processor element, the last-named one processor
5 element outputs a switching request signal to said
6 control section for switching said processor elements
7 from said last-named one processor element to the
8 last-named another processor element.

1 5. A multiprocessor system according to claim 3,
2 wherein said switching request signal is a switching
3 control interruption signal.

1 6. A multiprocessor system according to claim 4,
2 wherein said switching request signal is a switching
3 control interruption signal.

1 7. A multiprocessor system according to claim 1,
2 wherein, upon receipt of a signal from outside said
3 system, said control section outputs an interruption
4 signal to the last-named another processor element

5 to stop the performance thereof.

1 8. A multiprocessor system according to claim 2,
2 wherein, upon receipt of a signal from outside said
3 system, said control section outputs an interruption
4 signal to said another processor element to stop the
5 performance thereof.

1 9. A multiprocessor system according to claim 3,
2 wherein, upon receipt of a signal from outside said
3 system, said control section outputs an interruption
4 signal to said last-named another processor element
5 to stop the performance thereof.

1 10. A multiprocessor system according to claim 4,
2 wherein, upon receipt of a signal from outside said
3 system, said control section outputs an interruption
4 signal to said last-named another processor element
5 to stop the performance thereof.

1 11. A multiprocessor system according to claim 5,
2 wherein, upon receipt of a signal from outside said
3 system, said control section outputs an interruption
4 signal to said last-named processor element to stop
5 the performance thereof.

1 12. A multiprocessor system according to claim 6,

2 wherein, upon receipt of a signal from, said control
3 section outputs an interruption signal to said
4 last-named processor element to stop the performance
5 thereof.

1 13. A multiprocessor system according to claim 1,
2 wherein said control section has a table for indicating,
3 for designation of one at a time from said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 14. A multiprocessor system according to claim 2,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 15. A multiprocessor system according to claim 3,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor

5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 16. A multiprocessor system according to claim 4,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 17. A multiprocessor system according to claim 5,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 18. A multiprocessor system according to claim 6,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor

5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 19. A multiprocessor system according to claim 7,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform
5 processor element, which is allowed to perform
6 processing, and controls the switching of said
7 processor elements so as to designate said
8 permitted-to-perform processor element based on
9 said table.

1 20. A multiprocessor system according to claim 8,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 21. A multiprocessor system according to claim 9,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural

4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 22. A multiprocessor system according to claim 10,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 23. A multiprocessor system according to claim 11,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural
4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 24. A multiprocessor system according to claim 12,
2 wherein said control section has a table for indicating,
3 for designation of one at a time among said plural

4 processor elements, a permitted-to-perform processor
5 element, which is allowed to perform processing, and
6 controls the switching of said processor elements so
7 as to designate said permitted-to-perform processor
8 element based on said table.

1 25. A multiprocessor system according to claim 13,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 another processor element, and outputs an interruption
6 signal to said permitted-to-perform processor element
7 to stop the performance thereof.

1 26. A multiprocessor system according to claim 14,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 another processor element, and outputs an interruption
6 signal to said permitted-to-perform processor element
7 to stop the performance thereof.

1 27. A multiprocessor system according to claim 15,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an

6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 28. A multiprocessor system according to claim 16,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 29. A multiprocessor system according to claim 17,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 30. A multiprocessor system according to claim 18,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 31. A multiprocessor system according to claim 19,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 32. A multiprocessor system according to claim 20,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 33. A multiprocessor system according to claim 21,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 34. A multiprocessor system according to claim 22,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor

4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 35. A multiprocessor system according to claim 23,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 36. A multiprocessor system according to claim 24,
2 wherein, with consulting said table, said control
3 section selects said permitted-to-perform processor
4 element, which is indicated by said table, as said
5 last-named another processor element, and outputs an
6 interruption signal to said permitted-to-perform
7 processor element to stop the performance thereof.

1 37. A multiprocessor system according to claim 1,
2 wherein said control section actuates one of said
3 plural processor elements with precedence over the
4 remaining processor elements, and actuates one of said
5 remaining processor elements in place of the
6 second-to-last-named one processor element as demand

7 arises.

1 38. A multiprocessor system according to claim 1,
2 wherein said plural processor elements are different
3 in function from one another.

1 39. A multiprocessor system according to claim 38,
2 wherein, upon receipt of a signal from outside said
3 system, said control section selects, from said plural
4 processor elements, one processor element to handle
5 the last-named signal, and actuates the selected one
6 processor element.

1 40. A multiprocessor system according to claim 38,
2 wherein at least one of said plural processor element
3 is an MPU (Micro Processing Unit) and the remainder
4 is a DSP (Digital Signal Processor), or vice versa.

1 41. A multiprocessor system according to claim 39,
2 wherein at least one of said plural processor element
3 is an MPU (Micro Processing Unit) and the remainder
4 is a DSP (Digital Signal Processor), and vice versa.

1 42. A multiprocessor system according to claim 1,
2 further comprising an invalidating section for
3 invalidating the switching function of said control
4 section to thereby actuate at least two or more of

5 said plural processor elements simultaneously.

1 43. A multiprocessor system according to claim 1,
2 wherein said handover information to be stored in said
3 storing section includes at least one selected from
4 the group consisting of a value of a program counter,
5 an argument of a function, a return value of a function,
6 and content of a stack pointer.

1 44. A multiprocessor control method for switching two
2 or more processor elements of a multiprocessor system,
3 whose performances are to be executed by a common
4 program, said control method comprising the steps of:

5 (a) in response to each switching of said processor
6 elements, storing handover information relating to
7 the common program, which information is to be handed
8 over from said one processor element to said another
9 processor element, into a storing section of said
10 multiprocessor system; and

11 (b) after said handover information has been
12 stored into the storing section, stopping the
13 performance of said one processor element and starting
14 said another processor element using said handover
15 information stored in the storing section.

1 45. A computer-readable recording medium in which a
2 multiprocessor control program for switching two or

3 more processor elements of a multiprocessor system,
4 whose performances are to be executed by a common
5 program, wherein said multiprocessor control program
6 instructs a computer at the system to execute the steps
7 of:

8 (a) in response to each switching of said processor
9 elements, storing handover information relating to
10 the common program, which is to be handed over from
11 said one processor element to said another processor
12 element into a storing section of said multiprocessor
13 system; and

14 (b) after said handover information has been
15 stored into the storing section, stopping the
16 performance of said one processor element and stopping
17 the performance of said another processor element
18 using said handover information stored in said storing
19 section.